CES 530 – Microelectronics
PROJECT PROGRESS REPORT

David Bozarth
Engineering Science Department
Sonoma State University
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During our in-class project presentation session, we discussed methods for determining

- design values for the resistor and the MOSFET channels
- all node voltages and channel currents
- g_m and r_o for each transistor
- amplifier voltage gain, input resistance, and output resistance

At that time I had been struggling with basic circuit configuration using Multisim, and the simulation was not working. Subsequent work enabled me to achieve the connectivity of an amplifier, but its function was not correct.

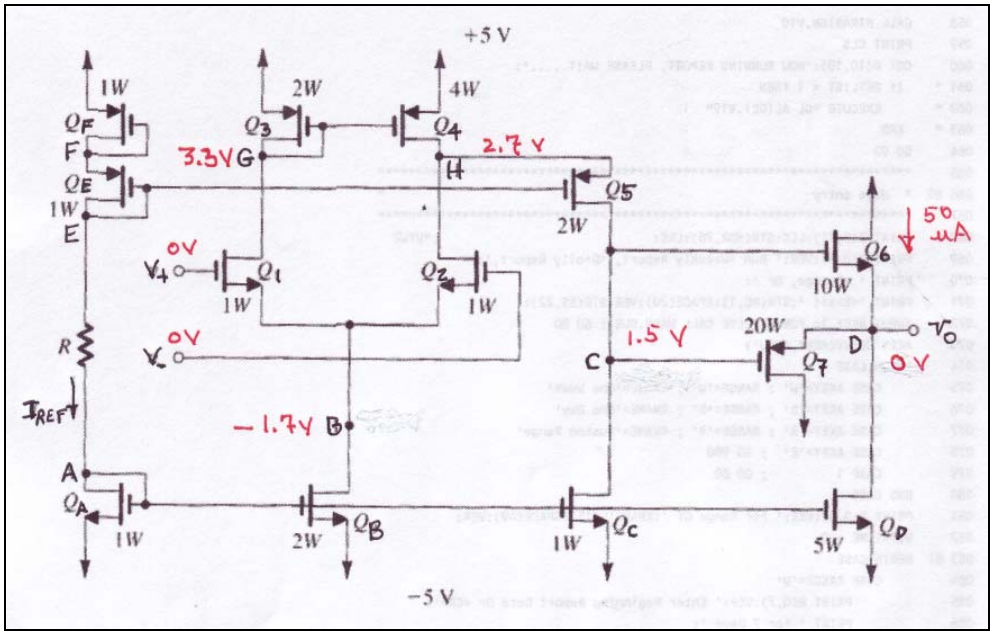

Figure 1. Amplifier schematic with selected DC design values.

The voltage at point C (*Figure 1*) was about ¼ volt, instead of the desired 1.5 volts. Since point C biases the active load Q_6, this arrangement was not suitable for a zero-volt DC level at the output node D. Also, point H was at 2.75 V rather than 2.70 V. Moreover, these voltages were independent of the components in the output stage being connected or not.

I wanted to eliminate the possibility that some hidden connectivity problem was dragging down point C. So I checked all component specs and rebuilt the simulation from scratch, placing and setting up the components before carefully connecting them.

Again the voltage at point C was about ¼ volt, and point H was 2.75 V. I re-checked all component values and connections, and concluded that either the design as presented in the problem statement was wrong, or Multisim would not render the correct DC performance for the given design. I reviewed the analysis of circuit voltages and currents determined by CMOS channel parameters, finding no discrepancy. Apparently there was some assumption being made in the design that was not validated by the simulation.

I experimented with changing the channel width-to-length ratio of Q_5. I found that when the voltage at point C was 1.5 V as desired, the ratio of k-values specified in Multisim for Q_5 vs. Q_C was about 1.2 ($k_5 / k_C = 1.2$) rather than the design ratio ($k_5 / k_C = 1$). So I altered k_5 to make point H be 2.7 V, then altered k_C to make ($k_5 / k_C = 1.2$) so that point C would be at 1.5 V.

At this point all DC voltages matched the design specifications (*Table 1*).

device	Design					Actual
	W/L	I_D, µA	V_{GS}	g_M, µmho	r_O, MΩ	W/L
Q_A	1	10	1.7	28.6	5.0	1
Q_B	2	20	1.7	57.1	2.5	2
Q_C	1	10	1.7	28.6	5.0	0.98
Q_D	5	50	1.7	142.9	1.0	5
Q_E	1	10	-2.0	20.0	5.0	1
Q_F	1	10	-2.0	20.0	5.0	1
Q_1	1	10	1.7	28.6	5.0	1
Q_2	1	10	1.7	28.6	5.0	1
Q_3	2	10	-1.7	28.6	5.0	2
Q_4	4	20	-1.7	57.1	2.5	4
Q_5	2	10	-1.7	28.6	5.0	2.35
Q_6	10	50	1.5	200.0	1.0	10
Q_7	20	0	1.5	0.0	∞	20

Table 1. Component design values with actual W/L required for DC operating point.

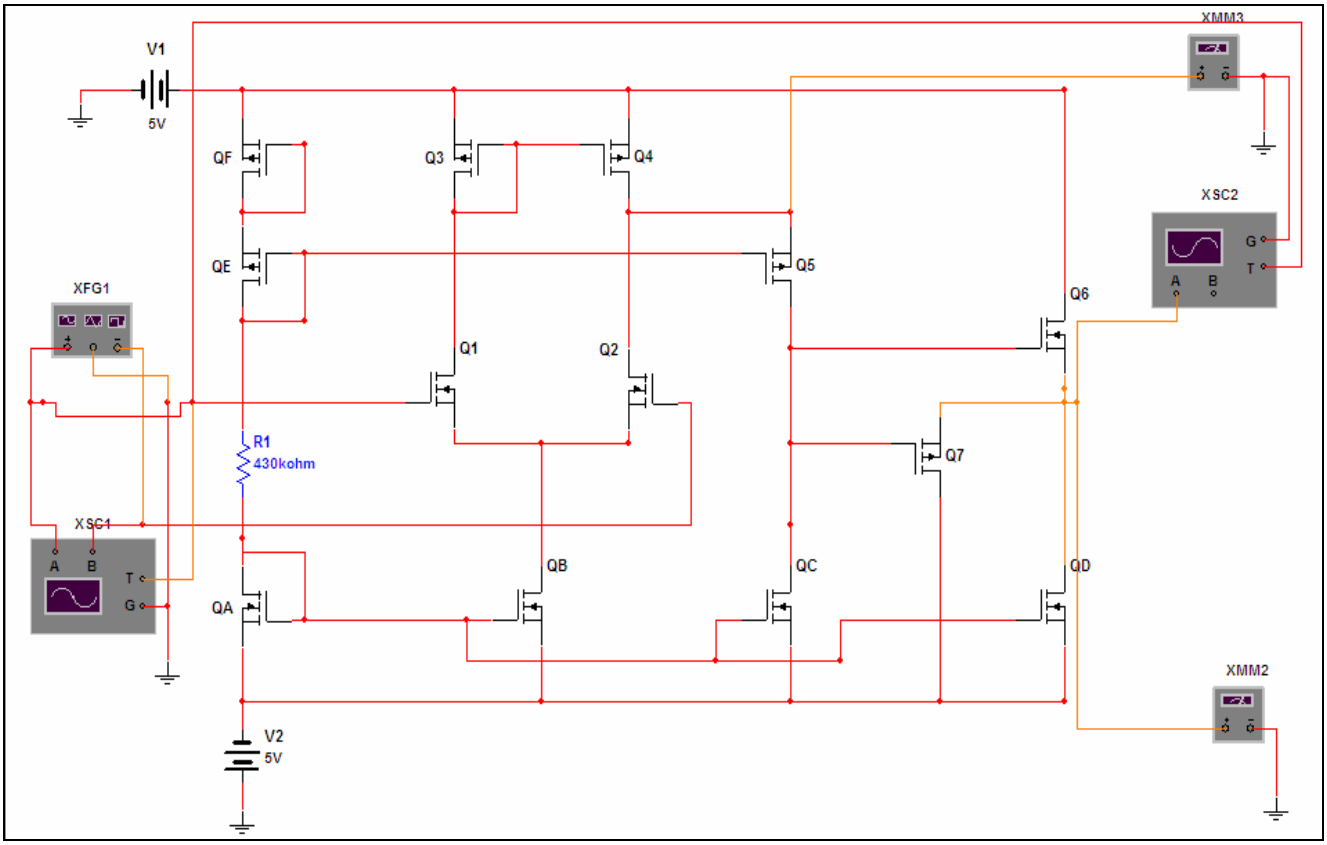

Figure 2. Working amplifier with modified W/L ratio for Q_5, Q_C

Signal Characteristics

I added a signal generator, 2 oscilloscopes, and some multimeters to the layout (*Figure 2*). I started with a single-ended 1 mV p-p, 1 KHz sinusoidal test signal, and applied the same (non-inverted and inverted) signal to both differential inputs. I measured the amplifier voltage gain (*Figure 3*), unity-gain bandwidth, input resistance, and output resistance.

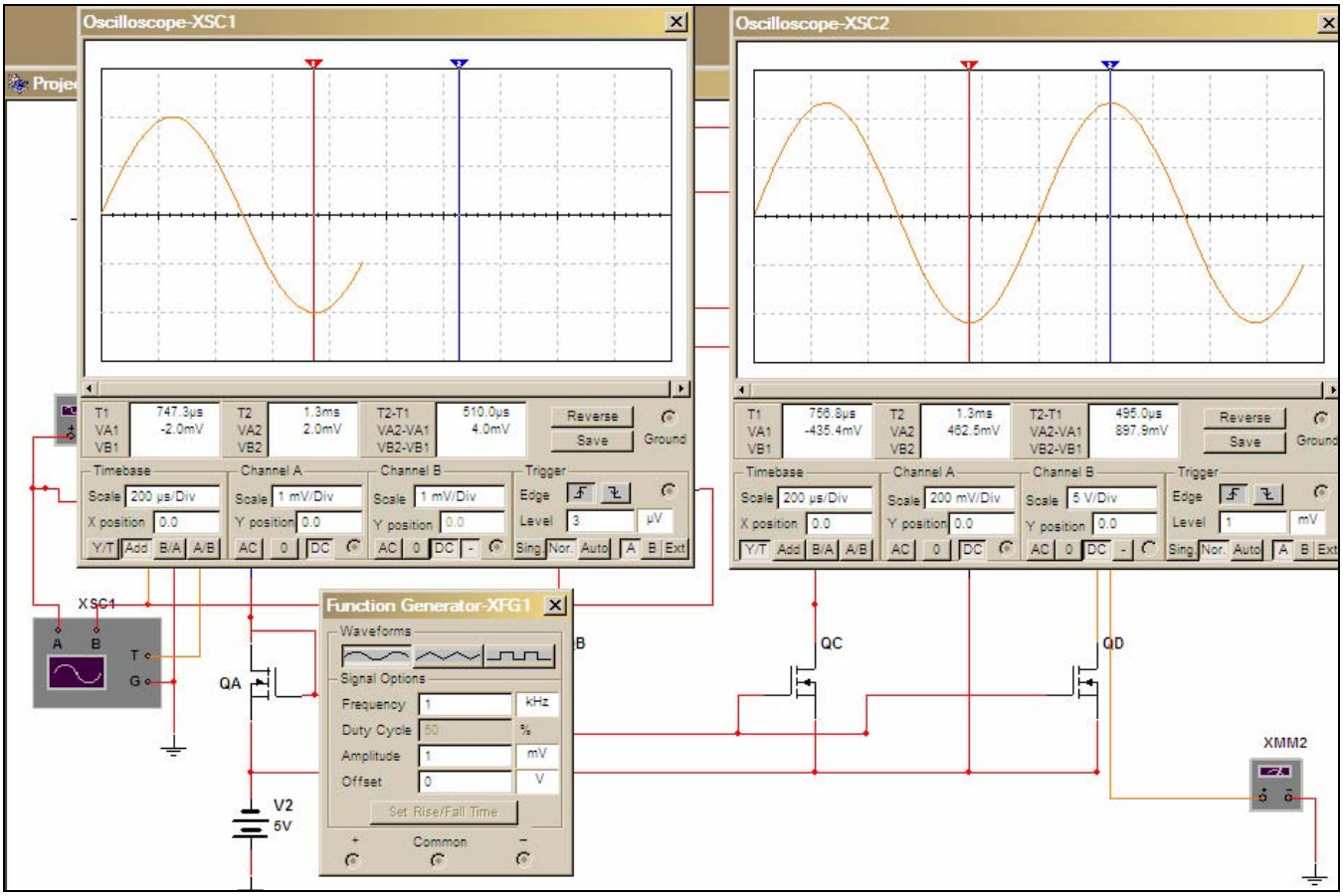

Figure 3. Amplifier voltage gain measurement

For this test signal, the amplifier voltage gain magnitude was found to be 224. (The output trace is shown inverted; the sign of the voltage gain is actually negative.) During the class presentation, we decided the voltage gain magnitude should be close to 130. Since this is open-loop gain, what we care about is that the magnitude be as large as possible.

I compared the stage gains to those we decided on during the presentation. The gain of the input stage, measured at point H, was found to be about -2.9 (theoretical gain of this stage was about -48). The gain of the common-base stage, measured at point C, was found to be about 77 (theoretical gain of this state was 2.6). So the amplifier appears to behave quite differently from prediction in terms of gain. (I did confirm that multimeter loading was not affecting stage gain or overall gain.)

Interestingly, points H and C were those whose DC voltages were tweaked into compliance by modifying the current gains of Q_5 and Q_C. I decided to connect an ammeter to find the actual current through point C. With inputs grounded, this current was about 11 µA (10% greater than the design value).

So a conjecture is that by changing the channel geometries of Q_C and Q_5, I also changed the stage and overall signal gain characteristics of the amplifier.

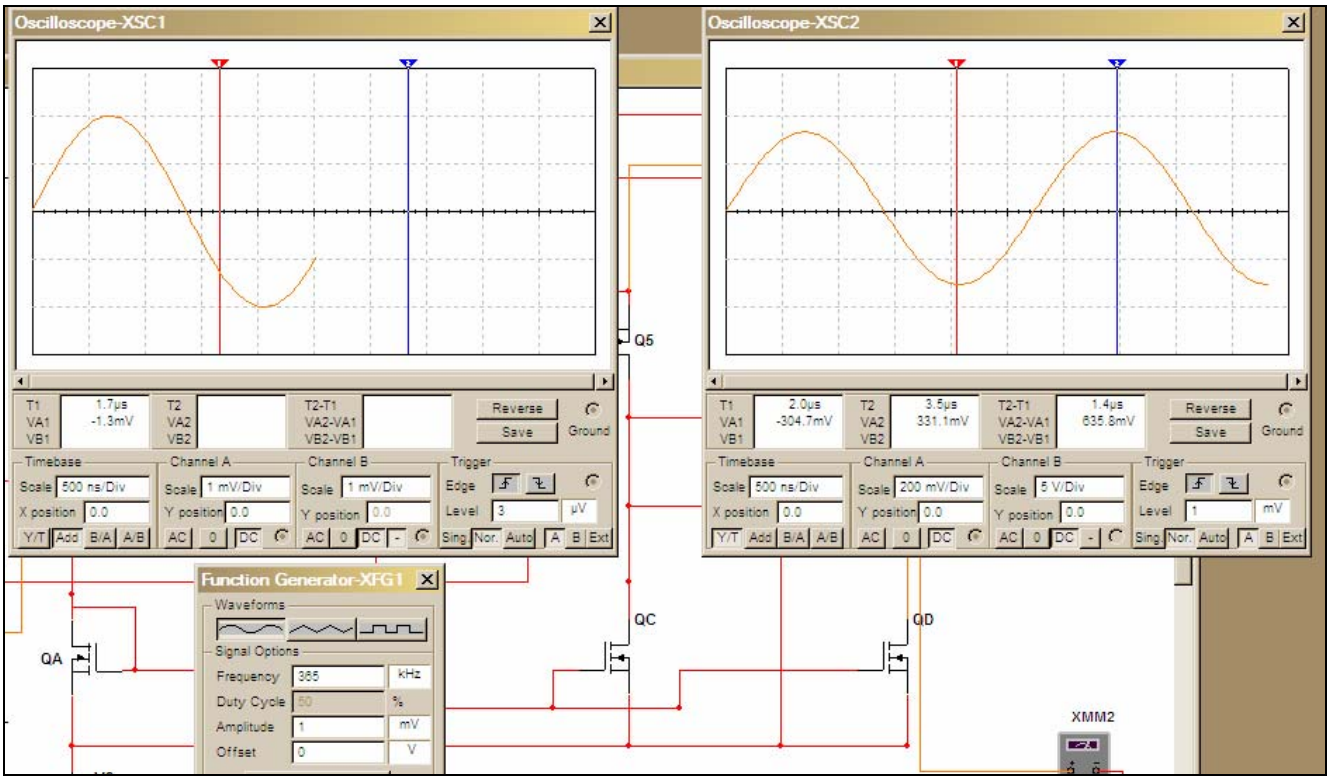

Figure 4. Unity-gain bandwidth measurement.

By increasing the generator frequency until the voltage gain was reduced by a factor of √2, I found the unity-gain bandwidth to be 365 KHz (*Table 2, Figure 4*).

In order to find input resistance, I monitored the RMS current flowing into each of the differential inputs, noted that their polarities were as expected, and divided the sum of their magnitudes into the RMS voltage across the differential input (*Figure 5*).

	theory	0.75 mV	1.0 mV	dynamic
Rin, MΩ	∞	10.1	13.5	∞
Rout, KΩ	5	2.58	2.87	4.34

Table 2. Input and output resistance

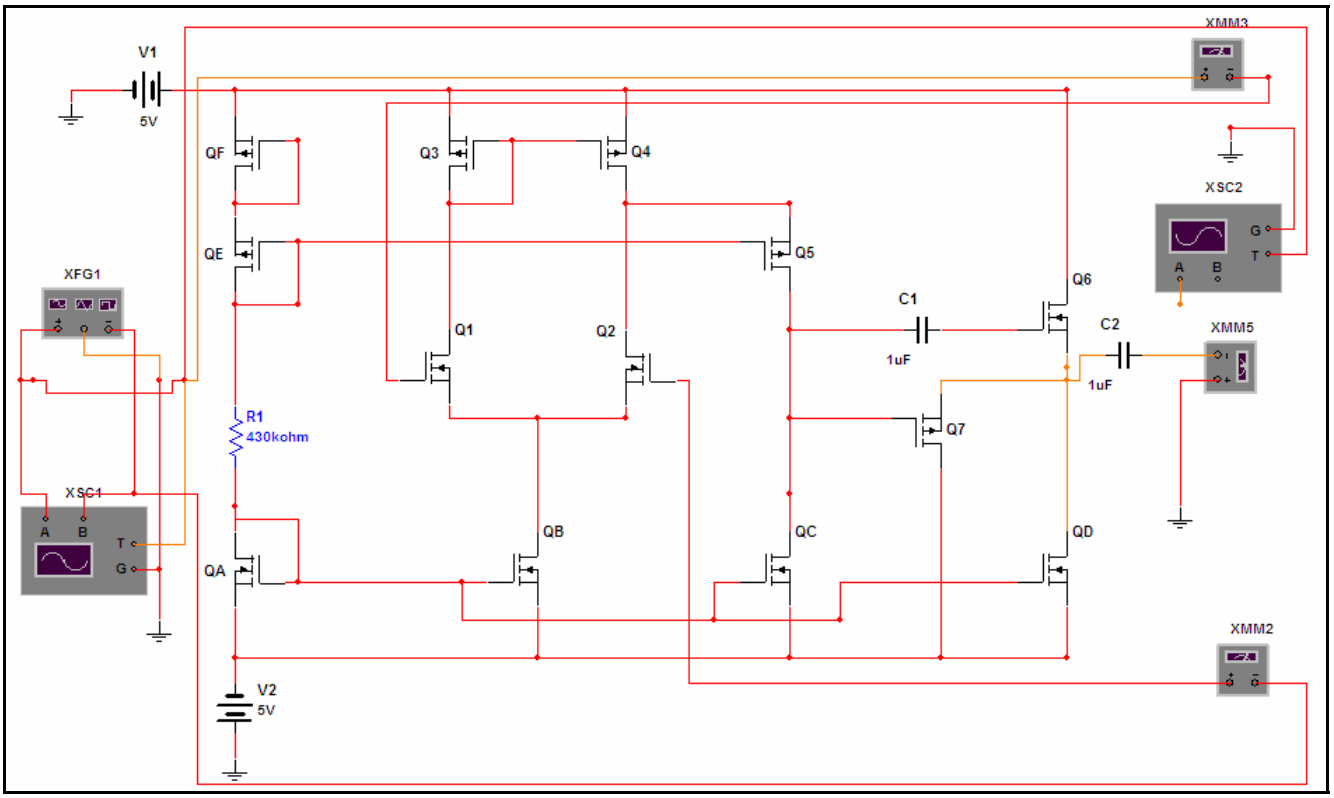

Figure 5. Setup for measuring input and output resistance.

To find output resistance, I placed a capacitor in series with the output node (point D). To measure open circuit voltage, I connected the free end of the capacitor to the oscilloscope input. To measure short-circuit current, I connected the free end of the capacitor in series with a grounded ammeter (*Figure 5*). I took the ratio of RMS voltage to RMS current as the output resistance.

I used two different amplitudes of input signal, found the amplifier's input and output resistance for each input level, then calculated the dynamic resistance $(v_2 - v_1) / (i_2 - i_1)$. For both input and output, dynamic resistance rendered the best agreement with theory.